NEW UTILITY PATENT APPLICATION TRANSMITTAL

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First Named Inventor (or Identifier)	WU et al.
Total Pages	17

This submits a new application under 37 CFR 1.53(b).

Entitled: A NEW METHOD OF DIGITAL FM DEMODULATOR

☒ 1. Submitted herewith are the following:

_6_ pages of specification, including an Abstract,
_3_ sheet(s) of drawings, and
_8_ claim(s).

☒ 2. Submitted herewith is an Oath/Declaration signed by each inventor.

☐ 3. Submitted herewith are the following:
- ☐ __ signed Independent Inventor Small Entity Statement(s),
- ☐ __ signed Small Business Small Entity Statement(s),
- ☐ __ signed Non-Profit Small Entity Statement(s).
- ☐ __ signed Non-Inventor Small Entity Statement(s),

☐ 4. A preliminary amendment is enclosed.

☐ 5. Submitted herewith is an Information Disclosure Statement, ___ pages of Form PTO-1449, and one copy of each document listed thereon.

☒ 6. An assignment of the invention to National Science Council of Republic of China.

☐ 7. A certified copy of application no. _____ in _____.

☒ 8. The Commissioner is authorized to credit any over payment and charge any deficiency in any fees required under 37 CFR 1.16, 1.17 and/or 1.18, to Deposit Account No. 02-0200.

☒ 9. A check in the amount of $ 800.00 is submitted herewith.

☐ 10. Other:_____

THE FILING FEE IS CALCULATED AS FOLLOWS:				Basic Fee:	$760.00
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Independent Claims:	3	- 3 =	0	X $78 =	$0.00
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				Subtotal:	$760.00
				50% Reduction if Small Entity Status:	
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June 7, 1999	Eugene Mar		25,893

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A New Method Of Digital FM Demodulator

BACKGROUND OF THE INVENTION

1.Field of the invention

The present invention relates to a new method of digital frequency-modulation demodulator , and more particularly, to a digital frequency-modulation demodulator that using the structure of time-to-digital converter and the concept of delta-sigma analog-to-digital converter .

2.Description Of The Prior Art

The frequency modulation (FM) is one of important and common method in radio communication system that its receiver end contains the FM demodulation circuit which often using analog design circuit and the conventional analog style FM demodulation circuit including detector circuit and phase lock loop circuit . If bring the detector into integrated circuit then it need bigger chip area, and if implement PLL into integrated circuit then an external capacitor is necessary outside this chip .

If the modulated signal need the digital signal process after demodulation , then the above two circuit need analog-to-digital converter to convert the demodulated analog signal into digital signal , meanwhile, this analog signal is easy to be interfered by noise signal . However, the digital FM demodulator will first convert the modulation intermediate-frequency (IF) signal into digital signal by way of analog-to-digital converter, then using digital signal processor to demodulate this modulation signal . The analog-to-digital converter and digital signal processor used in digital FM demodulator must have fast speed to demodulate the modulation signal in real time . It also could use reference clock with multiple-fold frequency of modulation signal for sampling the input modulation signal to detect its phase change then demodulate, but such technology need a high frequency reference clock .

The conventional methods of digital RF communication system always need to convert the analog signal into digital signal in the receiver end with drawbacks that increasing the circuit complexity . Thus, the demodulation circuit combines the detector circuit or PLL with analog-to-digital circuit could simply the circuit design also will be one of major objectives today .

SUMMARY OF THE INVENTION

It is therefore a primary objective of the present invention to provide a new method of digital FM demodulator will be applicable in radio communication system, besides, the modulation-demodulation section in receiver end also could be applicable in BB call , cellular phone , GPS system , and DECT system .

The next objective of the present invention is to provide a digital FM demodulator with two function of modulation-demodulation and analog-to-digital conversion ◦ The input intermediate-frequency signal pass through this invention demodulator will generate a digital signal including high-frequency quantized signal ， then by way of a low-pass filter to filter out above quantized noise signal to get the basedband signal ◦

The other objective of the present invention is to provide a digital FM demodulator which adopt the PLL structure and utilize the concept of delta-sigma analog-to-digital converter which without connect external component and high frequency reference clock so that easy for integration ◦

This invention with advantages that not only use delay lines as the timing reference but also adopt the concept of delta-sigma analog-to-digital converter to achieve the time-to-digital conversion for digital FM demodulator ◦ This digital FM demodulator including delay lines ， m-to-1 multiplexer ， phase detector ， charge pump circuit ， quantizer and digital integrator ◦ The modulation signal in intermediate frequency segment pass through the delay lines with the delay time around one cycle time ， and this delayed signal compare its phase with original signal ◦ This compared pulse will go through charge pump circuit and convert into a voltage level stored in capacitor ◦ This quantized voltage is accumulated by the digital integrator, then sample another output signal of delay lines and compare phase with input signal ◦ This system is similar to PLL , is a feedback system ◦ The quantized digital signal will feed through low-pass filter to filter out high frequency noise and get the original modulation signal, this modulation signal is a digital signal ◦

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings disclose an illustrative embodiment of the present invention Which serves to exemplify the various advantages and objects hereof, and are as follows:

Fig.1 is the circuit block diagram of digital FM demodulator according to the present invention ◦

Fig.2 is the circuit waveform of digital FM demodulator according to the present invention ◦

Fig.3 is the system structure of digital FM demodulator according to the present invention ◦

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Please refer to Fig.1 that relates to the circuit block diagram of digital FM demodulator ◦ The modulation signal Ai(t) is fed into reference delay lines 11 ﹐ said reference delay lines-11 including coarse delay line 111 and fine delay line 112 ﹐ those delay time of delay lines 111 and 112 is controlled separately by other circuits ◦ The fine delay lines 112 has multiple output signal Ai1(t),Ai2(t),Ai3(t)..... Aij(t) which could be expressed as follow:

$Aij(t)=Ai(t-Tc-j*\tau)$ ----- (1)

Tc: the total fixed delay time of coarse delay lines

τ : the unit delay time of fine delay lines

The phase detector compares the phase difference between Aid and Ai,then generate up and down signal.The m-to-1 multiplexer will select one of output signal Ai0(t), Ai1(t),Ai2(t) ---- Aij(t) from fine delay lines 112 and name it as Aid signal ◦ If the rising edge of Aid signal lead the Ai signal ﹐ up signal will generate an effective pulse and its pulse width is just same as the time difference between the rising edges of Ai and Aid, but down signal do not genarate any effective pulse ◦ The total delay time of Ai signal pass through delay lines is "Tc+d* τ ", and the pulse width will equal to "T-Tc-d* τ " when "Tc+d* τ " smaller than period T of Ai signal ◦

In the same way ﹐ if the rising edge of Aid signal lag the Ai signal ﹐ down signal will generate an effective pulse and its pulse width is also just same as the time difference of Aid and Ai signal, and the pulse width will equal to "Tc+d* τ -T" ◦

Its value is positive when Aid lead the Ai signal, on the contrary, its value is negative when Aid lag Ai signal ◦ Both effective pulse of up and down signal will trigger the charge pump circuit 14 for charging and discharging to capacitor Cc which will generate a voltage difference $\triangle Vf$ ﹐ and its voltage level is proportional to the time difference or phase difference of Aid and Ai signal ◦

Each cycle of input modulated signal will generate a $\triangle Vf$ which is accumulated in stored capacitor Cc and this stored voltage will be quantized to generate a bit stream digital signal y(k), y(k) is the output digital sequence of total system ◦

Quantizer 15 is a analog-to-digital converter which could be one bit or multiple bit converter ◦ One bit converter is the comparator ﹐ The quantizer 15 in this invention adopt one bit voltage comparator ◦

Digital integrator 16 accumulate output digital signal y(k), actually, it is simply an up-down counter due to quantizer 15 is one bit analog-digital converter ◦ The counter output signal will select one output Aid signal from the fine delay lines by way of multiplexer and compare its phase with Ai

signal ◦ Consequently ， the delay time of Aid signal is controlled by output signal y(k) ， it will delay one more unit time if y(k)=1 ， On the contrary ， the delay of Aid decrease one unit delay if y(k)=0 ◦ Thus ， this whole system is similar to PLL structure ， Y(K) is feedback to adjust the Aid delay time and make the next rising edge of Ai signal arrive phase detector with rising edge of Aid signal simultaneously ， so the Aid signal is just delayed one cycle than Ai signal when the system is locked ◦

As shown in Fig.2 ， this is the circuit waveform of digital FM demodulator according to the present invention ◦ T(k) is the kth cycle time of input modulation signal and P(k) is the time difference of Aid rising edge with next Ai cycle ◦ The effective pulse of up signal means P(k) is positive value ， but the down signal make P(K) negative ◦ That is because the maximum frequency shift of input modulation signal is much smaller than carrier frequency ◦ The change of T(k) is small relative to carrier cycle Tc ◦

Therefore ， the effective pulse of up signal and down signal only happen at rising edge of Aid and Ai signal ， and this effective pulse has been transferred to $\triangle Vf$ that is stored in capacitor Cc by way of charge pump circuit before arriving of falling edge ◦ This falling edge could be the trigger clock of the quantizer and counter ，

That means this system do not need external reference clock ◦ As shown in Fig.2 waveform diagram ， a formula as follows :

$P(k+1)=P(k)+T(k)-T(k-1)+y(k)*\tau$ ------ (2)

Definition:

$\triangle T(k)=T(k)-T(k-1)$ ------ (3)

Therefore, we could get;

$P(k+1)=P(k)+\triangle T(k)+y(k)*\tau$ ------ (4)

If V(k) means the capacitor voltage at kth cycle ， based on Fig.2, we could see V(k) signal is generated by V(k-1) and Ic signal to charge/discharge Cc during up or down signal effective pulse period and Ib charge/discharge Cc during kth cycle ， i.e. the voltage is determined by these three parameters ◦

The voltage on Cc for Ic at kth cycle is :

$\triangle Vf\_a=Ic/Cc*P(k)$ ------ (5)

If the trigger clock is the input modulation signal Ai ， then the Cc voltage level will be next formula when charge-discharge is at kth cycle ◦

$\triangle Vf\_b=y(k)*Ib/Cc*[T(k)+T(k+1)]/2$ ------ (6)

Then

$\triangle Vf=\triangle Vf\_a+\triangle Vf\_b$ ------ (7)

$V(k+1)=V(k)+\{y(k)*(Ib/Cc)*[T(k)+T(k+1)]/2\}+\{Ic/Cc*P(k)\}$ ------(8)

Because the maximum frequency shift is much smaller than carrier frequency , the T(k) is around equal to carrier cycle Tc .

$$V(k+1)=V(k)+Ic/Cc*P(k)+y(k)*(Ib/Cc)*Tc \quad \text{----- (9)}$$

Assume

$A=Ic/Cc$;

$B=(Ib/Cc)*Tc$

We could get next formula :

$V(k+1)=V(k)+A*P(k+1)+B*y(k)$

Put the P(k+1) into above formula, then get

$$V(k+1)=V(k)+A*[P(k)+\Delta T(k)+y(k)*\tau]+B*y(k)$$

The quantized output of V(k) is the total system output .

As shown in Fig.3 , is the system structure of digital FM demodulator according to the present invention . This diagram is a two level delta-sigma structure , its input is $\Delta T(k)$ that also is the signal difference of T(k) and T(k-1) .

The concept of the output signal y(k) in present invention is similar to conventional analog-digital converter output signal , the quantized noise signal is shifted to high frequency segment . So , the output digital signal y(k) is accumulated first then filter out quantized noise by the digital filter to get the modulation signal .

These technology is similar to conventional delta-sigma analog-to-digital converter . Based on above deduction , the output digital signal is the differentiation of original modulation signal . In brief , y(k) signal filter out the quantized noise by way of low-pass digital filter before signal accumulation .

This invention provide a FM digital demodulator which with more advantages than conventional technology as follow:

1. the method and circuit in present invention will be applicable in radio communication system, besides, the modulation-demodulation section in receiver end also could be applicable in BB call , cellular phone , GPS system , and DECT system .

2. the present invention to provide a digital modulation demodulator which adopt the PLL structure and utilize the concept of delta-sigma analog-to-digital converter which without connect external component and high frequency reference clock so that easy for integration .

3. the present invention to provide a digital modulation demodulator with two function of demodulation and analog-to-digital conversion ◦ The input of intermediate-frequency signal pass through this invention demodulator will generate a digital signal including high-frequency quantized signal ◦ then by way of low-pass filter to filter out above quantized noise signal to get the basedband signal ◦

Many changes and modifications in the above described embodiment of the invention can, of course, be carried out without departing from the scope thereof. Accordingly, to promote the progress in science and the useful arts, the invention is disclosed and is intended to be limited only by the scope of the appended claims.

CLAIMS

What is claimed is:

1. A new method of digital FM demodulator , comprising:
   a. input the modulation signal to the delay lines with multiple output;
   b. select one output signal from the multiple output delay lines;
   c. compare the delayed signal phase with original modulation signal and accumulate each compared phase difference;
   d. said accumulated phase difference is quantized into one or more bit digital signal;
   e. generate another set of digital signal based on the above accumulated digital signal;
   f. re-select output signal from the multiple output delay lines according to the signal generated in step-e;
   g. repeat the phase comparison and accumulation in step-c ◦ and quantization in step-d ◦ digital accumulation in step-e and re-select output signal from the multiple output delay lines in step-f ◦ again the step-c,d,e,f;
   h. After one cycle of step c-d-e-f ◦ there is one set of digital signal pass to integrator and filter out the quantized noise by way of a low-pass filter to get the original modulation signal ◦

2. A new method of digital FM demodulator as claimed in claim 1, wherein said phase difference could convert into voltage or current waveform for accumulation and quantization ◦

3. A new method of digital FM demodulator , comprising:
   a. delay input modulation signal by digital controlled delay lines;
   b. compare the delayed rising or falling edge of modulation signal with the original modulation signal by phase detector to generate the phase-leading or phase-lagging pulse signal;

c. convert the phase difference of said two pulse into voltage level and stored in capacitor ，the voltage difference accumulated in capacitor is equal to the phase difference accumulation;
d. quantize the capacitor voltage into one or more bit digital signal;
e. integrate or accumulate the digital signal by digital integrator to generate another set of digital signal;
f. put the output signal of digital integrator into the digital controlled delay lines to control the delay time of delayed modulation signal;
g. do a cycle of step b,c,d,e to accumulate a digital signal will generate another set of digital signal which will filter out the high frequency quantized noise by a low-pass filter to get original modulation signal 。

4. A new method of digital FM demodulator , comprising:
a. a digital controlled delay lines used to delay input modulation signal;
b. a phase detector to generate phase-leading or phase-lagging signal based on the rising or falling edge of delayed modulation signal compared with original modulation signal;
c. a capacitor store the accumulation voltage difference ，said accumulated voltage is also the accumulation of the phase difference;
d. a quantized one or more bit digital signal from capacitor voltage;
e. a digital integrator to accumulate the said above digital signal to generate another set of digital signal;
f. a output digital signal from said integrator to delay lines to control the delay time of delayed modulation signal;
g. a quantizer which output signal been filter our by a low-pass filter to get the original modulation signal 。

5. A new method of digital FM demodulator as claimed in claim 4, wherein said digital controlled delay lines comprising delay units, multiplexer, and decoder; each output of delay unit is relative to each input of multiplexer and the delay time of each delay unit is the same; the input digital signal after decoding could select the corresponding output signal of multiplexer; therefore, the delay time of digital controlled delay lines is determined by input digital signal 。

6. A new method of digital FM demodulator as claimed in claim 4, wherein the quantizer and digital integrator need a trigger signal that could use input modulation signal directly; said phase detector will compare the rising edge of input modulation signal and delayed modulation signal and using the falling edge to trigger said quantizer and integrator 。

7. A new method of digital FM demodulator as claimed in claim 4, wherein the said quantizer could be one or more bit analog-to-digital converter and one bit quantizer is a voltage comparator 。

8. A new method of digital FM demodulator as claimed in claim 4, wherein the said quantizer and integrator use same bit number and one bit integrator is a up-down counter ◦

ABSTRACT OF THE DISCLOSURE

The present invention relates to a new method of digital FM demodulator that using the delay lines as timing reference and the concept of delta-sigma analog-to-digital converter to implement the function of time-to-digital conversion; said FM demodulator comprising delay lines, multiplexer, phase detector, charge pump circuit, quantizer and digital integrator ◦ The modulation signal in intermediate frequency segment will pass through delay lines around one cycle time and compare with original input modulation signal, and the compared pulse converted into voltage and store in capacitor by way of charge pump circuit ◦ The quantized voltage has been accumulated, then re-select a new delayed output signal to compare its phase with input signal ◦ This system is similar to PLL, is a feedback system ◦ This quantized digital signal again pass through a low-pass filter to filter out high frequency qnantized noise to get the original digital modulation signal ◦

This invention combines the function of demodulation and analog-to-digital conversion ◦

標號意義英譯[圖式標號說明]

11 delay lines
111 coarse delay lines
112 fine delay lines
12 m-to-1 multiplexer
13 phase detector
14 charge and discharge circuit
15 quantizer
16 digital integrator

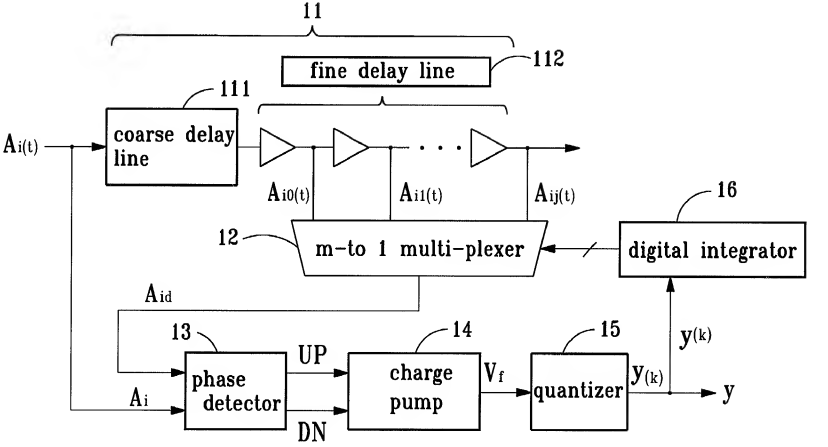

FIG. 1

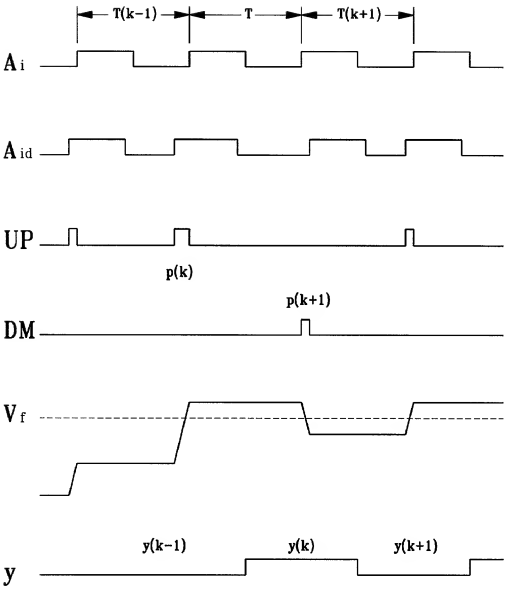

FIG.2

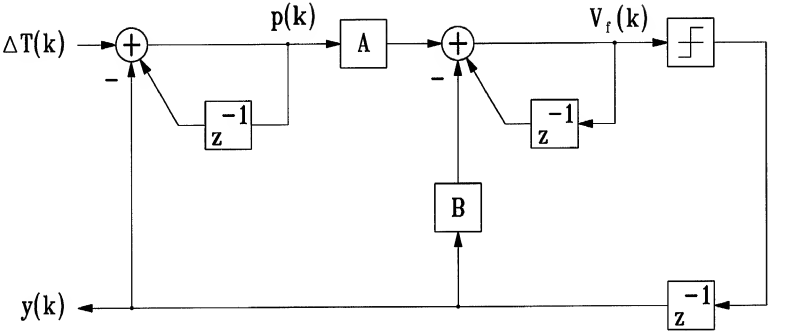

FIG.3

PATENT

Docket No. _____.

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence , post office address, and citizenship are as stated below under may name. I believe I am the sole (if only one name appears below), or a joint (if more than one name appears), original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **A New Method of Digital FM Demodulator**

_____.

x The specification for the above entitled invention is filed herewith.

____The specification for the above entitled invention was filed previously with application serial number_____, filed on_____.

I hereby state I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56 (a).

PRIORITY CLAIM

x There is no claim of priority.

____Claim of priority is based on the following:

_____.

_____.

_____.

POWER OF ATTORNEY

As a named inventor , I hereby appoint the following attorney to prosecute this application and to transact all related business in the Patent and Trademark Office:

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I authorize my attorney to accept and follow instructions from Asian Pacific Int'l Patent & Trademark Office regarding any matter related to this application or any patent that my issue from this application. This authorization shall remain valid until such time as I may revoke it in writing.

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United Stated Code and that such willful false statements may jeopardize the validity of the application or any patent issued hereon. I hereby acknowledge the duty in any continuation-in-part application to disclose to the Patent and Trademark Office all information known to be material, as defined in § 1.56, which application and the filing date of this application.

Date: 5-17-1999

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